COMPUTER ORGANIZATION AND DESIGN
The Hardware/Software Interface
5th Edition

Chapter 2

Other Instruction Sets

The Intel x86 ISA

- Evolution with backward compatibility
  - 4004 (1971): Intel invents the microprocessor
  - 8080 (1974): 8-bit microprocessor
    - Accumulator, plus 3 index-register pairs
  - 8086 (1978): 16-bit extension to 8080
    - Complex instruction set (CISC)
  - 8087 (1980): floating-point coprocessor
    - Adds 60 floating point instructions, 80-bit FP registers
  - 80286 (1982): 24-bit addresses, MMU
    - Segmented memory mapping and protection
  - 80386 (1985): 32-bit extension (now IA-32)
    - Additional addressing modes and operations
    - Paged memory mapping as well as segments

The Intel x86 ISA

- Further evolution…
  - i486 (1989): pipelined, on-chip caches and FPU
    - Compatible competitors: AMD, Cyrix, …
  - Pentium (1993): superscalar, 64-bit datapath
    - Later versions added MMX (Multi-Media eXtension) instructions
    - The infamous FDIV bug (read text book)
  - Pentium Pro (1995), Pentium II (1997)
    - New microarchitecture (see Colwell - *The Pentium Chronicles*)
    - 57 new instructions
    - Primarily for multimedia applications (SIMD)
  - Pentium III (1999)
    - Added SSE (Streaming SIMD Extensions) and associated registers
    - Four 32-bit floating point operations in parallel
    - Useful in speech recognition, video encoding/decoding

The Intel x86 ISA

- And further…
  - Pentium 4 (2001) – Itanium
    - New microarchitecture - IA-64 (RISC-like) architecture
    - Added SSE2 instructions
    - Explicitly Parallel Instruction Computing (EPIC)
    - 128-bit bundle with three instructions and a template
    - 128 general purpose registers and 128 floating point registers
    - Done by a partnership between HP and Intel
    - Able to run both UNIX and Microsoft Windows
  - AMD64 (2003): extended architecture to 64 bits
    - Increases address space to 64 bits
    - Widens all registers to 64 bits
    - Other changes (AMD64)
  - EM64T – Extended Memory 64 Technology (2004)
    - AMD64 adopted by Intel (with refinements)
    - Added SSE3 instructions

The Intel x86 ISA

- Further yet …
  - Intel Core (2006)
    - Added SSE4 instructions, virtual machine support
  - AMD64 (announced 2007): SSE5 instructions
    - Intel declined to follow, instead…
  - Advanced Vector Extension (announced 2008)
    - Longer SSE registers, more instructions
- If Intel didn't extend with compatibility, its competitors would!
  - Technical elegance ≠ market success

The Intel x86 ISA Conclusions

- Conclusion (Hennessy and Patterson):
  - "This history illustrates the impact of the "golden handcuffs" of compatibility".
  - "Adding new features as someone might add clothing to a packed bag".
  - "An architecture that is difficult to explain and impossible to love".

Implementing IA-32

- Complex instruction set makes implementation difficult:
  - Hardware translates instructions to simpler micro-operations:
    - Simple instructions: 1 – 1.
    - Complex instructions: 1 – many.
  - Microengine similar to RISC.
- Comparable performance to RISC:
  - Compilers avoid complex instructions.

ARM & MIPS Similarities

- ARM: the most popular embedded core.
- Similar basic set of instructions to MIPS.

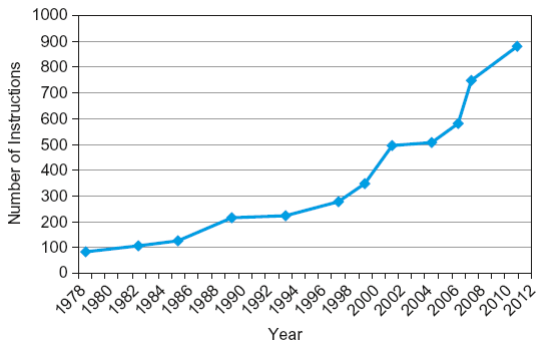
	ARM	MIPS
Date announced	1985	1985
Instruction size	32 bits	32 bits
Address space	32-bit flat	32-bit flat
Data alignment	Aligned	Aligned
Data addressing modes	9	3
Registers	15 × 32-bit	31 × 32-bit
Input/output	Memory mapped	Memory mapped

ARM v8 Instructions

- In moving to 64-bit, ARM did a complete overhaul.
- ARM changes from v7 (v8 resembles MIPS):
  - No conditional execution field;
  - Immediate field is a 12-bit constant;
  - Dropped load/store multiple;
  - PC is no longer a General Purpose Register (GPR);
  - GPR set expanded to 32;
  - Addressing modes work for all word sizes;
  - Divide instruction;
  - Branch if equal/branch if not equal instructions.

Fallacies

- Backward compatibility ⇒ instruction set doesn't change
  - But they do accrete more instructions.

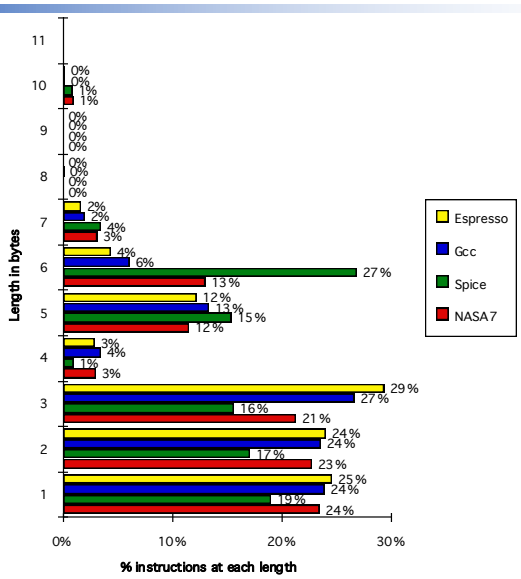


x86 instruction set

Top 10 80x86 Instructions

Rank	instruction	Integer Average
1	load	22%
2	conditional branch	20%
3	compare	16%
4	store	12%
5	add	8%
6	and	6%
7	sub	5%
8	move register-register	4%
9	call	1%
10	return	1%
	Total	96%

80x86 Instruction Length Distribution



Fallacies

- Powerful instruction ⇒ higher performance
  - Fewer instructions required.
  - But complex instructions are hard to implement
    - May slow down all instructions, including simple ones.
  - Compilers are good at making fast code from simple instructions.
- Use assembly code for high performance
  - Modern compilers are better at dealing with modern processors.
  - More lines of code ⇒ more errors and less productivity.

Concluding Remarks

- Design principles:
  1. Simplicity favors regularity;
  2. Smaller is faster;
  3. Make the common case fast;
- MIPS: typical of RISC ISAs